REMARKS

An Office Action was mailed August 4, 2008 and was declared final. An Advisory Action was mailed December 5, 2008. This response is timely. Any fee due with this paper, including any necessary extension fees, may be charged on Deposit Account 50-1290.

Summary

Claims 1, 3, 11, 13, and 21 are pending; other claims are cancelled or withdrawn. Claims 1, 11, and 21 are the only independent claims.

By the foregoing, all independent claims are amended, and new claims are presented. No new matter has been added.

Rejection under 35 U.S.C. §103(a)

Claims 1, 3, 11, and 13 stand rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,232,945 to Moriyama in view of U.S. Patent No. 6,734,840 to Fukutofu. Claim 21 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Moriyama in view of Fukutofu and JP 2001-349643 to Hirobumi.

With respect to independent claims 1 and 11, Moriyama is cited for teaching all claimed limitation except that the polarity of the data voltage applied to each of the pixels "*is not inverted after each horizontal synchronizing period*." Fukutofu is cited to fill the gap. It is suggested JP 2001-349643 to Hirobumi also teaches this limitation.

With respect to claim 21, Moriyama is cited for teaching all claimed limitations. However, Moriyama does not teach that the polarity is inverted in every set of two horizontal synchronizing periods, e.g., 2-H dot inversion method. Moriyama also does not teach that the polarity is inverted in every set of two horizontal synchronizing periods, e.g., 2-H dot inversion method. Hirobumi is cited to fill the gap.

All independent claims now claim that:

the source driver has a resetting means for resetting the data voltages outputted by the source driver circuit exclusively throughout a blanking period of each of the horizontal synchronizing periods of the set.

Support thereof may be found in the specification, as filed, on pg. 31, line 16 et al., see also Fig. 7.,

"Thereafter, the latching operation is started at the rising edge t3 of the signal STB . . . [s]ubsequently, the latching operation thus started is ended at the next falling edge t4 of the signal STB. This means that the image data in the circuit 141 is latched within the period from the time t3 to the time t4 in which the signal STB is kept in its high level (H)" Emphasis added.

As Fig. 7 makes clear, the resetting occurs throughout the period t3 and t4, which corresponds to the blanking period, T.sub.B. Advantageously, by using the entire banking period a gradual voltage resetting operation is permitted.

In contrast, Moriyama teaches that a delay of time, delta.t, occurs before the reset signal is given. See Figs. 6, 7, 9, and 11 and col. 8, line 28 et al. Thus, the resetting operation is more abrupt and made in a shorter time period. Consequently, damage to the pixel element may more readily occur.

Indeed, Moriyama needs the time delay to select desired display areas without processing the video signal. Col. 9:21 et al. Moriyama teaches that the display device may have display area 502 and non-display areas 503 and 504. Thus, images of 4:3 may be displayed on a 16:9 screen. Col. 8, line 3 et al. The black display potential, e.g., non-displayed data, may be written in the pixel electrodes 151 corresponding to the non-display areas 503, 504. This occurs during the blanking period. If it were not for the time delay, delta.t, during the blanking period the TFT would be controlled by a time constant of scanning line.

Neither Fukutofu nor Hirobumi fill this gap in Moriyama to arrive at the presently claimed invention. Fukutofu is silent as to any blanking period being utilized to reset the voltage. Hirobumi according to an automatic translation from the Japanese Patent Office website

(courtesy copy enclosed, an Information Disclosure Statement being filed therewith) is equally silent with using the blanking period.

In contrast, Hirobumi teaches that the time for resetting, e.g., reducing the gate voltage from a high level to a low level occurs during a horizontal synchronizing period is simultaneous to the time when the gate voltage is increased from a low level to a high level in a subsequent synchronizing period.

In the presently claimed invention, when the resetting occurs is earlier than when the voltage is increased in the next period. In other words, the resetting occurs only, e.g., exclusively, during the blanking period and throughout e.g., is continuous during, the blanking period.

None of the references individually or in a combination of references teaches, discloses, or suggests the claimed invention. Accordingly, the Examiner is respectfully requested to withdraw the rejection.

In view of the remarks set forth above, this application is believed to be in condition for allowance which action is respectfully requested. However, if for any reason the Examiner should consider this application not to be in condition for allowance, the Examiner is respectfully requested to telephone the undersigned attorney at the number listed below prior to issuing a further Action.

Any fee due with this paper may be charged to Deposit Account No. 50-1290.

Respectfully submitted,

_/Hassan A. Shakir/_____
Hassan A. Shakir
Reg. No. 53,922
212.940.6489

CUSTOMER NUMBER 026304
Docket No.: NECA 20.522 (100806-00219)